EAST SEARCH

12/21/05

L#	Hits	Search String	Databases
S1	3374	((Integrated or digital) near2 circuit$1) and netlist	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S2	99	S1 and (edit$3 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S3	348	S1 and (netlist$1 with module$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S4	587	S1 and (netlist$1 with (chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S5	3	S1 and (netlist$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S6	820	S1 and (netlist$1 with ("hardware description language" or HDL or VHDL or verilog))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S7	579	S1 and (netlist$1 with ("hardware description language" or VHDL or verilog))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S8	193	S1 and (netlist$1 with object$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S9	758	S1 and (netlist$1 with element$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S10	558	S1 and (netlist$1 with representation$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S11	1	S1 and (netlist$1 with representational)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S12	10	S1 and (netlist$1 with compliler)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S13	185	S1 and (module with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S14	141	S1 and (configuration with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S15	114	S1 and (wire with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S16	445	S1 and (netlist$1 with (hierarchical or hierarchy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S17	167	S1 and (netlist$1 with (hierarchical or hierarchy) with level$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S18	146	S1 and (instance with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S19	2	S1 and (instance with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S20	2	S1 and (element$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S21	1	S1 and (attribute$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S22	1	S1 and (port$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S23	201	S1 and (port$1 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S24	3	S1 and (object-based with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S25	100	S3 and S4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S26	80	S3 and S7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S27	57	S3 and S8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S28	127	S3 and S9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S29	132	S3 and S10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S30	23	S13 and S14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S31	111	S3 and S13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S32	11	S3 and S14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S33	24	S13 and S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S34	50	S3 and S17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S35	32	S13 and S18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S36	31	S3 and S18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S37	45	S13 and S23	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S38	388	S2 or S5 or S12 or S19 or S20 or S21 or S22 or S24 or S25 or S26 or S27 or S28 or S29 or S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S39	272	S2 or S5 or S12 or S19 or S20 or S21 or S22 or S24 or S26 or S27 or S30 or S32 or S33 or S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S40	349	S15 or S25 or S28 or S29 or S31	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S41	157	S39 and S40	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S42	272	S39 or S41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S43	3380	((Integrated or digital) near2 circuit$1) and netlist	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S44	1	S43 and (definitional with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S46	348	S43 and (netlist$1 with module$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S48	582	S43 and (netlist$1 with ("hardware description language" or VHDL or verilog))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S49	194	S43 and (netlist$1 with object$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S51	185	S43 and (module with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S52	141	S43 and (configuration with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S53	114	S43 and (wire with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S54	168	S43 and (netlist$1 with (hierarchical or hierarchy) with level$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S55	146	S43 and (instance with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S56	2	S43 and (instance with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S57	2	S43 and (element$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S58	1	S43 and (attribute$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S59	1	S43 and (port$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S60	202	S43 and (port$1 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S61	3	S43 and (object-based with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S62	80	S46 and S48	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S63	57	S46 and S49	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S64	23	S51 and S52	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S67	50	S46 and S54	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S69	31	S46 and S55	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S70	45	S51 and S60	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S71	272	S45 or S47 or S50 or S56 or S57 or S58 or S59 or S61 or S62 or S63 or S64 or S65 or S66 or :	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S72	588	S43 and (netlist$1 with (chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S73	761	**S43 and (netlist$1 with element$1)**	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S74	559	S43 and (netlist$1 with representation$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S75	100	S46 and S72	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S76	127	S46 and S73	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S77	132	S46 and S74	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S78	111	S46 and S51	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S79	349	S53 or S75 or S76 or S77 or S78	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S80	157	S71 and S79	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S81	272	S71 or S80	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S45	99	S43 and (edit$3 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S47	3	S43 and (netlist$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S50	10	S43 and (netlist$1 with compliler)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S65	11	S46 and S52	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S66	24	S51 and S53	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S68	32	S51 and S55	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S82	3382	((Integrated or digital) near2 circuit$1) and netlist	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S83	1	S82 and (definitional with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S84	99	S82 and (edit$3 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S85	348	S82 and (netlist$1 with module$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S86	3	S82 and (netlist$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S87	582	S82 and (netlist$1 with ("hardware description language" or VHDL or verilog))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S88	194	S82 and (netlist$1 with object$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S89	10	S82 and (netlist$1 with compliler)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S90	185	S82 and (module with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S91	141	S82 and (configuration with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S92	114	S82 and (wire with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S93	168	S82 and (netlist$1 with (hierarchical or hierarchy) with level$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S94	146	S82 and (instance with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S95	2	S82 and (instance with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S96	2	S82 and (element$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S97	1	S82 and (attribute$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S98	1	S82 and (port$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S99	202	S82 and (port$1 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S100	3	S82 and (object-based with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S101	80	S85 and S87	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S102	57	S85 and S88	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S103	23	S90 and S91	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S104	11	S85 and S91	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S105	24	S90 and S92	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S106	50	S85 and S93	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S107	32	S90 and S94	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S108	31	S85 and S94	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S109	45	S90 and S99	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S110	272	S84 or S86 or S89 or S95 or S96 or S97 or S98 or S100 or S101 or S102 or S103 or S104 or S	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S111	588	S82 and (netlist$1 with (chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S112	761	S82 and (netlist$1 with element$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S113	559	S82 and (netlist$1 with representation$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S114	100	S85 and S111	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S115	127	S85 and S112	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S116	132	S85 and S113	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S117	111	S85 and S90	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S118	349	S92 or S114 or S115 or S116 or S117	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S119	157	S110 and S118	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S120	272	S110 or S119	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S121	299	S82 and (wire with (chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S122	124	S82 and (port with (chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S123	8	S121 and S122	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S124	3	S82 and (wire with port with (chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S125	79	S82 and (attribute$1 with (chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S126	11	S82 and (attribute$1 with (netlist or element) with(chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S127	3564	((Integrated or digital) near2 circuit$1) and netlist	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S128	102	S127 and (edit$3 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S129	55	S128 and (edit$3 with schematic$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S130	32	S128 and (edit$3 with HDL)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S131	17	S129 and S130	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S132	63	S128 and HDL	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S133	3655	((Integrated or digital) near2 circuit$1) and netlist	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S134	104	S133 and (edit$3 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S135	32	S134 and (edit$3 with HDL)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S136	13	S134 and (netlist with version$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S137	0	S136 and ((several or plurality or multiple) with version$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S138	3	S134 and ((several or plurality or multiple) with version$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S139	0	S135 and ((several or plurality or multiple) with version$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S140	3655	((Integrated or digital) near2 circuit$1) and netlist	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S141	104	S140 and (edit$3 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S142	3	S141 and ((several or plurality or multiple) with version$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S143	5	S141 and ((modif$4 or chang$3) with netlist with version$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S144	4	S141 and ((modif$4 or chang$3) with netlist with module$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

10/032789 **John Walther**

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Results of search set S120

Document	Kind Codes	Title	Issue Date	Current OR	Abstract
US 20050137841	A1	Embedding keys into test data	20050623	703/14	
US 20050131666	A1	Circuit simulation bus transaction analysis	20050616	703/17	
US 20050125758	A1	Positioning of inverting buffers in a netlist	20050609	716/10	
US 20050108672	A1	Method of generating a physical netlist for a hierarchical integrated circuit design	20050519	716/12	
US 20050097493	A1	Gate reuse methodology for diffused cell-based IP blocks in platform-based silicon products	20050505	716/11	
US 20050091627	A1	Comparison of two hierarchical netlist to generate change orders for updating an integrated circ	20050428	716/12	
US 20050080953	A1	Fragment storage for data alignment and merger	20050414	710/52	
US 20050080952	A1	Descriptor-based load balancing	20050414	710/52	
US 20050078696	A1	Descriptor write back delay mechanism to improve performance	20050414	370/419	
US 20050078694	A1	Packet manager interrupt mapper	20050414	370/412	
US 20050078669	A1	Exponential channelized timer	20050414	370/389	
US 20050078601	A1	Hash and route hardware with parallel routing scheme	20050414	370/218	
US 20050050506	A1	System and method for determining connectivity of nets in a hierarchical circuit design	20050303	716/12	
US 20050050488	A1	System and method for determining a highest level signal name in a hierarchical VLSI design	20050303	716/4	
US 20050038928	A1	Distributed configuration storage	20050217	710/8	
US 20050033870	A1	Distributed configuration storage	20050210	710/8	

US 20050027491 A1	Symbolic analysis of electrical circuits for application in telecommunications	20050203	702/196
US 20040230920 A1	Method and apparatus for implementing engineering change orders	20041118	716/1
US 20040225490 A1	Device for emulating one or more integrated-circuit chips	20041111	703/27
US 20040207429 A1	Semiconductor integrated circuit and circuit design apparatus	20041021	326/40
US 20040194048 A1	System and method for efficiently mapping heterogeneous objects onto an array of heterogeneo	20040930	716/17
US 20040186703 A1	System and method for estimating power consumption for at least a portion of an integrated circ	20040923	703/18
US 20040163067 A1	Method and apparatus for layout of high speed digital logic for datapath portions of microprocess	20040819	716/10
US 20040158789 A1	Using pseudo-pins in generating scan test vectors for testing an embedded core while maintaini	20040812	714/741
US 20040128641 A1	Simplified process to design integrated circuits	20040701	716/18
US 20040128626 A1	Placement of configurable input/output buffer structures during design of integrated circuits	20040701	716/1
US 20040123258 A1	Logic multiprocessor for FPGA implementation	20040624	716/5
US 20040122990 A1	Distributed configuration storage	20040624	710/8
US 20040117756 A1	Methods and apparatuses for designing integrated circuits	20040617	716/18
US 20040115995 A1	Circuit array module	20040617	439/701
US 20040111252 A1	Method and system for emulating a design under test associated with a test environment	20040610	703/28
US 20040073876 A1	Method and apparatus for enhancing the performance of event driven dynamic simulation of digi	20040415	716/6
US 20040025136 A1	Method for designing a custom ASIC library	20040205	716/17
US 20040021490 A1	Method and apparatus for timing management in a converted design	20040205	327/165
US 20040002846 A1	Transistor level verilog	20040101	703/19
US 20030229872 A1	Simulation result verification method and simulation result verification device	20031211	716/6
US 20030229870 A1	Systems and methods for performing clock gating checks	20031211	716/6
US 20030208721 A1	Apparatus and method to facilitate hierarchical netlist checking	20031106	716/1
US 20030204822 A1	Digital logic optimization using selection operators	20031030	716/2
US 20030200510 A1	Digital circuits using universal logic gates	20031023	716/1
US 20030200070 A1	Simulation of uncharacterized hardware	20031023	703/14
US 20030188268 A1	Low Vt transistor substitution in a semiconductor device	20031002	716/2
US 20030177457 A1	Optimization of digital designs	20030918	716/3
US 20030177427 A1	Circuit modeling	20030918	714/741
US 20030149954 A1	Methods and apparatuses for designing integrated circuits	20030807	716/18
US 20030149953 A1	Integrated circuit cell library	20030807	716/17
US 20030149859 A1	Digital circuit implementation by means of parallel sequencers	20030807	712/21
US 20030145288 A1	Method and apparatus for improving digital circuit design	20030731	716/2
US 20030139842 A1	Fast algorithm to extract flat information from hierarchical netlists	20030724	700/182
US 20030126579 A1	Digital design using selection operations	20030703	716/18
US 20030125925 A1	Batch editor for netlists described in a hardware description language	20030703	703/22
US 20030121013 A1	Timing model extraction by timing graph reduction	20030626	716/6
US 20030120474 A1	Assertion handling for timing model extraction	20030626	703/19
US 20030101331 A1	ASIC design technique	20030529	712/36
US 20030084416 A1	Scalable, partitioning integrated circuit layout system	20030501	716/7
US 20030084410 A1	SPICE to Verilog netlist translator	20030501	716/3
US 20030079195 A1	Methods and apparatuses for designing integrated circuits	20030424	716/8
US 20030079192 A1	METHOD FOR GENERATING A PARTITIONED IC LAYOUT	20030424	716/7
US 20030033595 A1	Automated HDL modifying apparatus and computer-readable recording medium in which prograi	20030213	717/143
US 20030014703 A1	Using pseudo-pins in generating scan test vectors for testing an embedded core while maintaini	20030116	714/726

US 20030009734 A1	Method for generating design constraints for modules in a hierarchical integrated circuit design s	20030109	716/6
US 20030009727 A1	Circuit designing apparatus, circuit designing method and timing distribution apparatus	20030109	716/1
US 20020194575 A1	Hierarchical layout method for integrated circuits	20021219	716/17
US 20020194572 A1	Methods and apparatuses for designing integrated circuits	20021219	716/1
US 20020183997 A1	Apparatus and method for specifying the configuration of mixed-language simulation models	20021205	703/13
US 20020170037 A1	Apparatus and method for controlling event ordering in a mixed- language simulator	20021114	717/131
US 20020166110 A1	Apparatus and method for performing event processing in a mixed-language simulator	20021107	717/106
US 20020156609 A1	Circuit simulation method, circuit simulation device, and circuit simulation program and compute	20021024	703/14
US 20020147576 A1	System for characterizing simulated circuit logic and behavior	20021010	703/15
US 20020145433 A1	An algorithm for finding vectors to stimulate all paths and arcs through an LVS gate	20021010	324/530
US 20020138817 A1	Method for inserting antenna diodes into an integrated circuit design	20020926	716/12
US 20020129334 A1	Interface based design using a tabular paradigm	20020912	717/123
US 20020083398 A1	Circuit designing apparatus, circuit designing method and timing distribution apparatus	20020627	716/1
US 20020073380 A1	Block based design methodology with programmable components	20020613	716/1
US 20020045995 A1	Electromagnetic interference analysis method and apparatus	20020418	702/77
US 20020038401 A1	Design tool for systems-on-a-chip	20020328	710/305
US 20020023107 A1	Schematic organization tool	20020221	715/504
US 20020018583 A1	Advanced schematic editor	20020214	382/113
US 20010047509 A1	Modular design method and system for programmable logic devices	20011129	716/18
US 20010034873 A1	Device level layout optimization in electronic design automation	20011025	716/8
US 20010001881 A1	Methods and media for utilizing symbolic expressions in circuit modules	20010524	716/1
US 6915410 B2	Compiler synchronized multi-processor programmable logic device with direct transfer of compu	20050705	712/17
US 6904571 B1	Algorithm and methodology for the polygonalization of sparse circuit schematics	20050607	716/2
US 6892373 B2	Integrated circuit cell library	20050510	716/17
US 6886140 B2	Fast algorithm to extract flat information from hierarchical netlists	20050426	716/1
US 6877150 B1	Method of transforming software language constructs to functional hardware equivalents	20050405	716/18
US 6876961 B1	Electronic system modeling using actual and approximated system properties	20050405	703/19
US 6872601 B1	Method and apparatus for timing management in a converted design	20050329	438/129
US 6868534 B2	Circuit modeling	20050315	716/6
US 6868531 B1	Generation of ordered interconnect output from an HDL representation of a circuit	20050315	716/1
US 6865726 B1	IC layout system employing a hierarchical database by updating cell library	20050308	716/18
US 6857110 B1	Design methodology for merging programmable logic into a custom IC	20050215	716/4
US 6856950 B1	Abstract verification environment	20050215	703/13
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US 6845494 B2	Method for generating design constraints for modules in a hierarchical integrated circuit design s	20050118	716/6
US 6836877 B1	Automatic synthesis script generation for synopsys design compiler	20041228	716/18
US 6823502 B2	Placement of configurable input/output buffer structures during design of integrated circuits	20041123	716/9
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US 6792589 B2	Digital design using selection operations	20040914	716/18
US 6792579 B2	Spice to verilog netlist translator and design methods using spice to verilog and verilog to spice t	20040914	716/3
US 6779158 B2	Digital logic optimization using selection operators	20040817	716/3
US 6779156 B2	Digital circuits using universal logic gates	20040817	716/1
US 6769107 B1	Method and system for implementing incremental change to circuit design	20040727	716/16
US 6745371 B2	Low Vt transistor substitution in a semiconductor device	20040601	716/2

US 6745358 B1	Enhanced fault coverage	20040601	714/726
US 6738957 B2	Schematic organization tool	20040518	716/11
US 6721926 B2	Method and apparatus for improving digital circuit design	20040413	716/2
US 6697982 B2	Generating netlist test vectors by stripping references to a pseudo input	20040224	714/738
US 6684373 B1	Optimize global net timing with repeater buffers	20040127	716/6
US 6678871 B2	Circuit designing apparatus, circuit designing method and timing distribution apparatus	20040113	716/6
US 6675366 B1	System and method for disabling schematics	20040106	716/11
US 6671868 B1	Method of creating MCM pinouts	20031230	716/16
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US 6658628 B1	Developement of hardmac technology files (CLF, tech and synlib) for RTL and full gate level netl	20031202	716/1
US 6651235 B2	Scalable, partitioning integrated circuit layout system	20031118	716/7
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US 6625787 B1	Method and apparatus for timing management in a converted design	20030923	716/6
US 6618834 B2	Circuit designing apparatus, circuit designing method and timing distribution apparatus	20030909	716/2
US 6601024 B1	Code translation between hardware design languages	20030729	703/14
US 6591402 B1	System and method for performing assertion-based analysis of circuit designs	20030708	716/5
US 6578183 B2	Method for generating a partitioned IC layout	20030610	716/7
US 6578133 B1	MIMD array of single bit processors for processing logic equations in strict sequential order	20030610	712/21
US 6574787 B1	Method and apparatus for logic synthesis (word oriented netlist)	20030603	716/18
US 6574779 B2	Hierarchical layout method for integrated circuits	20030603	716/1
US 6557156 B1	Method of configuring FPGAS for dynamically reconfigurable computing	20030429	716/17
US 6557149 B2	Algorithm for finding vectors to stimulate all paths and arcs through an LVS gate	20030429	716/4
US 6546536 B1	System and method for disabling schematics	20030408	716/11
US 6539536 B1	Electronic design automation system and methods utilizing groups of multiple cells having loop-t	20030325	716/18
US 6539520 B1	Systems and methods for generating hardware description code	20030325	716/3
US 6536028 B1	Standard block architecture for integrated circuit design	20030318	716/17
US 6536018 B1	Reverse engineering of integrated circuits	20030318	716/4
US 6530065 B1	Client-server simulator, such as an electrical circuit simulator provided by a web server over the	20030304	716/4
US 6526554 B1	Integrated circuit layout system, integrated circuit layout method, and computer-readable storage	20030225	716/10
US 6519755 B1	Method and apparatus for logic synthesis with elaboration	20030211	716/18
US 6519754 B1	Methods and apparatuses for designing integrated circuits	20030211	716/18
US 6519749 B1	Integrated circuit partitioning placement and routing system	20030211	716/9
US 6510548 B1	Method for providing pre-designed modules for programmable logic devices	20030121	716/16
US 6510546 B1	Method and apparatus for pre-routing dynamic run-time reconfigurable logic cores	20030121	716/16
US 6510542 B1	Method of placing a repeater cell in an electricalcircuit	20030121	716/10
US 6502229 B2	Method for inserting antenna diodes into an integrated circuit design	20021231	716/12
US 6499125 B1	Method for inserting test circuit and method for converting test data	20021224	714/734
US 6496955 B1	Latch mapper	20021217	716/3
US 6493864 B1	Integrated circuit block model representation hierarchical handling of timing exceptions	20021210	716/18
US 6493648 B1	Method and apparatus for logic synthesis (inferring complex components)	20021210	702/119

US 6490717 B1	Generation of sub-netlists for use in incremental compilation	20021203 716/18
US 6480995 B1	Algorithm and methodology for the polygonalization of sparse circuit schematics	20021112 716/11
US 6467074 B1	Integrated circuit architecture with standard blocks	20021015 716/17
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US 6446251 B1	Method and apparatus for socket-based design with reusable-IP	20020903 716/18
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US 6401231 B1	Method and apparatus for performing both negative and positive slack time budgeting and for de	20020604 716/6
US 6378123 B1	Method of handling macro components in circuit design synthesis	20020423 716/18
US 6374205 B1	Method of reducing circuit data, method of simulating circuit, and medium for storing circuit data	20020416 703/14
US 6366874 B1	System and method for browsing graphically an electronic design based on a hardware descripti	20020402 703/14
US 6360353 B1	Automated alternating current characterization testing	20020319 716/4
US 6360191 B1	Method and apparatus for automated design of complex structures using genetic programming	20020319 703/6
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US 6327556 B1	AT-speed computer model testing methods	20011204 703/13
US 6304837 B1	Automated test vector generation and verification	20011016 703/14
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US 6295636 B1	RTL analysis for improved logic synthesis	20010925 716/18
US 6292931 B1	RTL analysis tool	20010918 716/18
US 6292925 B1	Context-sensitive self implementing modules	20010918 716/8
US 6289498 B1	VDHL/Verilog expertise and gate synthesis automation system	20010911 716/18
US 6289491 B1	Netlist analysis tool by degree of conformity	20010911 716/5
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US 6243849 B1	Method and apparatus for netlist filtering and cell placement	20010605 716/8
US 6230304 B1	Method of designing a constraint-driven integrated circuit layout	20010508 716/7
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US 6216258 B1	FPGA modules parameterized by expressions	20010410 716/17
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US 6205572 B1	Buffering tree analysis in mapped design	20010320 716/5
US 6202044 B1	Concurrent hardware-software co-simulation	20010313 703/28
US 6182269 B1	Method and device for fast and accurate parasitic extraction	20010130 716/5
US 6175946 B1	Method for automatically generating checkers for finding functional defects in a description of a c	20010116 716/4
US 6173435 B1	Internal clock handling in synthesis script	20010109 716/18
US 6167555 A	System and method for converting polygon-based wires of an integrated circuit design to path-b:	20001226 716/3
US 6134705 A	Generation of sub-netlists for use in incremental compilation	20001017 716/18
US 6120549 A	Method and apparatus for generating optimized functional macros	20000919 703/20

US 6108494 A	Optimizing runtime communication processing between simulators	20000822 703/14
US 6106568 A	Hierarchical scan architecture for design for test applications	20000822 716/18
US 6102964 A	Fitting for incremental compilation of electronic designs	20000815 716/18
US 6080204 A	Method and apparatus for contemporaneously compiling an electronic circuit design by contemp	20000627 716/7
US 6078736 A	Method of designing FPGAs for dynamically reconfigurable computing	20000620 716/16
US 6067650 A	Method and apparatus for performing partial unscan and near full scan within design for test app	20000523 714/726
US 6064806 A	System and method for converting a polygon-based layout of an integrated circuit design to an o	20000516 716/3
US 6058252 A	System and method for generating effective layout constraints for a circuit design or the like	20000502 716/10
US 6014506 A	Method and apparatus for improving engineering change order placement in integrated circuit de	20000111 716/11
US 6002861 A	Method for performing simulation using a hardware emulation system	19991214 703/16
US 5991523 A	Method and system for HDL global signal simulation and verification	19991123 716/18
US 5983277 A	Work group computing for electronic design automation	19991109 709/232
US 5963454 A	Method and apparatus for efficiently implementing complex function blocks in integrated circuit d	19991005 716/18
US 5949692 A	Hierarchical scan architecture for design for test applications	19990907 716/18
US 5946478 A	Method for generating a secure macro element of a design for a programmable IC	19990831 716/17
US 5940603 A	Method and apparatus for emulating multi-ported memory circuits	19990817 716/5
US 5937179 A	Integrated circuit design system with shared hardware accelerator and processes of designing ir	19990810 716/16
US 5920830 A	Methods and apparatus for generating test vectors and validating ASIC designs	19990706 702/119
US 5903466 A	Constraint driven insertion of scan logic for implementing design for test within an integrated circ	19990511 716/18
US 5894420 A	Method for spawning two independent states in a state flow diagram	19990413 716/12
US 5875112 A	Methods for implementing circuit designs in physical circuits	19990223 716/12
US 5867397 A	Method and apparatus for automated design of complex structures using genetic programming	19990202 703/14
US 5857109 A	Programmable logic device for real time video processing	19990105 712/37
US 5850537 A	Pipe lined static router and scheduler for configurable logic system performing simultaneous con	19981215 716/12
US 5841663 A	Apparatus and method for synthesizing integrated circuits using parameterized HDL modules	19981124 716/18
US 5831869 A	Method of compacting data representations of hierarchical logic designs used for static timing ar	19981103 716/6
US 5831868 A	Test ready compiler for design for test synthesis	19981103 716/18
US 5828588 A	Parametrizable control module comprising first and second loadable counter, an electronic circui	19981027 708/273
US 5828579 A	Scan segment processing within hierarchical scan architecture for design for test applications	19981027 716/2
US 5812417 A	Method and apparatus utilizing datapath line minimization to generate datapath floor plan for inte	19980922 716/9
US 5812414 A	Method for performing simulation using a hardware logic emulation system	19980922 716/16
US 5805860 A	Methods, data structures and apparatus for traversing a hierarchical netlist	19980908 716/12
US 5805859 A	Digital simulator circuit modifier, network, and method	19980908 703/16
US 5796623 A	Apparatus and method for performing computations with electrically reconfigurable logic devices	19980818 703/23
US 5748875 A	Digital logic simulation/emulation system	19980505 714/29
US 5740071 A	Method and apparatus for selective shape adjustment of hierarchical designs	19980414 716/11
US 5734581 A	Method for implementing tri-state nets in a logic emulation system	19980331 703/15
US 5703789 A	Test ready compiler for design for test synthesis	19971230 716/4
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US 5691912 A	Method for entering state flow diagrams using schematic editor programs	19971125 716/11
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US 5661662 A	Structures and methods for adding stimulus and response functions to a circuit design undergoi	19970826 716/16

US 5659716 A	Pipe-lined static router and scheduler for configurable logic system performing simultaneous cor	19970819	703/23
US 5657241 A	Routing methods for use in a logic emulation system	19970812	716/16
US 5644498 A	Timing shell generation through netlist reduction	19970701	716/2
US 5633807 A	System and method for generating mask layouts	19970527	716/19
US 5625803 A	Slew rate based power usage simulation and method	19970429	703/14
US 5617327 A	Method for entering state flow diagrams using schematic editor programs	19970401	703/14
US 5612891 A	Hardware logic emulation system with memory capability	19970318	716/16
US 5603043 A	System for compiling algorithmic language source code for implementation in programmable har	19970211	712/1
US 5586319 A	Netlist editor allowing for direct, interactive low-level editing of netlists	19961217	716/17
US 5550839 A	Mask-programmed integrated circuits having timing and logic compatibility to user-configured lo	19960827	714/724
US 5541850 A	Method and apparatus for forming an integrated circuit including a memory structure	19960730	716/18
US 5535342 A	Pld connector for module having configuration of either first PLD or second PLD and reconfigura	19960709	710/315
US 5524244 A	System for dividing processing tasks into signal processor and decision-making microprocessor	19960604	717/140
US 5499192 A	Method for generating logic modules from a high level block diagram	19960312	716/17
US 5497498 A	Video processing module using a second programmable logic device which reconfigures a first p	19960305	710/104
US 5483461 A	Routing algorithm method for standard-cell and gate-array integrated circuit design	19960109	716/14
US 5471398 A	MTOL software tool for converting an RTL behavioral model into layout information comprising b	19951128	716/21
US 5452239 A	Method of removing gated clocks from the clock nets of a netlist for timing sensitive implementat	19950919	703/19
US 5452231 A	Hierarchically connected reconfigurable logic assembly	19950919	716/16
US 5448496 A	Partial crossbar interconnect architecture for reconfigurably connecting multiple reprogrammable	19950905	716/16
US 5422833 A	Method and system for propagating data type for circuit design from a high level block diagram	19950606	703/14
US 5402357 A	System and method for synthesizing logic circuits with timing constraints	19950328	716/12
US 5301318 A	Hierarchical netlist extraction tool	19940405	716/11
US 5287511 A	Architectures and methods for dividing processing tasks into tasks for a programmable real time	19940215	717/106
US 5200580 A	Configurable multi-chip module interconnect	19930406	174/264
US 5197016 A	Integrated silicon-software compiler	19930323	716/8
US 5197015 A	System and method for setting capacitive constraints on synthesized logic circuits	19930323	716/12
US 5187784 A	Integrated circuit placement method using netlist and predetermined ordering constraints to proc	19930216	716/7
US 5185736 A	Synchronous optical transmission system	19930209	370/358
US 5155836 A	Block diagram system and method for controlling electronic instruments with simulated graphic i	19921013	703/23
US 5111413 A	Computer-aided engineering	19920505	703/14
US 5036473 A	Method of using electronically reconfigurable logic circuits	19910730	703/23
US 4922432 A	Knowledge based method and apparatus for designing integrated circuits using functional specif	19900501	716/17
US 4868785 A	Block diagram editor system and method for controlling electronic instruments	19890919	345/440
US 6353915 B	Interconnected electronic components system evaluating method e.g. for circuit board assemblie	20020305	
US 5586319 A	Method of interactively editing netlist on computer - involves defining user commands, prompting	19961217	

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US 20050097493 A1	Gate reuse methodology for diffused cell-based IP blocks in platform-based silicon products	20050505	716/11
US 20040186703 A1	System and method for estimating power consumption for at least a portion of an integrated circ	20040923	703/18
US 20040163067 A1	Method and apparatus for layout of high speed digital logic for datapath portions of microprocess	20040819	716/10
US 20040021490 A1	Method and apparatus for timing management in a converted design	20040205	327/165
US 20030204822 A1	Digital logic optimization using selection operators	20031030	716/2
US 20030200510 A1	Digital circuits using universal logic gates	20031023	716/1

US 20030177457 A1	Optimization of digital designs	20030918 716/3
US 20030177427 A1	Circuit modeling	20030918 714/741
US 20030149953 A1	Integrated circuit cell library	20030807 716/17
US 20030149859 A1	Digital circuit implementation by means of parallel sequencers	20030807 712/21
US 20030145288 A1	Method and apparatus for improving digital circuit design	20030731 716/2
US 20030126579 A1	Digital design using selection operations	20030703 716/18
US 20030125925 A1	Batch editor for netlists described in a hardware description language	20030703 703/22
US 20030009727 A1	Circuit designing apparatus, circuit designing method and timing distribution apparatus	20030109 716/1
US 20020138817 A1	Method for inserting antenna diodes into an integrated circuit design	20020926 716/12
US 20020083398 A1	Circuit designing apparatus, circuit designing method and timing distribution apparatus	20020627 716/1
US 20010047509 A1	Modular design method and system for programmable logic devices	20011129 716/18
US 20010034873 A1	Device level layout optimization in electronic design automation	20011025 716/8
US 20010001881 A1	Methods and media for utilizing symbolic expressions in circuit modules	20010524 716/1
US 6957413 B1	System and method for specifying integrated circuit probe locations	20051018 716/18
US 6915410 B2	Compiler synchronized multi-processor programmable logic device with direct transfer of compu	20050705 712/17
US 6904571 B1	Algorithm and methodology for the polygonalization of sparse circuit schematics	20050607 716/2
US 6892373 B2	Integrated circuit cell library	20050510 716/17
US 6872601 B1	Method and apparatus for timing management in a converted design	20050329 438/129
US 6868534 B2	Circuit modeling	20050315 716/6
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US 6779156 B2	Digital circuits using universal logic gates	20040817 716/1
US 6721926 B2	Method and apparatus for improving digital circuit design	20040413 716/2
US 6678871 B2	Circuit designing apparatus, circuit designing method and timing distribution apparatus	20040113 716/6
US 6675366 B1	System and method for disabling schematics	20040106 716/11
US 6671866 B2	Device level layout optimization in electronic design automation	20031230 716/10
US 6634008 B1	Methodology server based integrated circuit design	20031014 716/1
US 6625787 B1	Method and apparatus for timing management in a converted design	20030923 716/6
US 6618834 B2	Circuit designing apparatus, circuit designing method and timing distribution apparatus	20030909 716/2
US 6578133 B1	MIMD array of single bit processors for processing logic equations in strict sequential order	20030610 712/21
US 6557156 B1	Method of configuring FPGAS for dynamically reconfigurable computing	20030429 716/17
US 6546536 B1	System and method for disabling schematics	20030408 716/11
US 6510546 B1	Method and apparatus for pre-routing dynamic run-time reconfigurable logic cores	20030121 716/16
US 6502229 B2	Method for inserting antenna diodes into an integrated circuit design	20021231 716/12
US 6480995 B1	Algorithm and methodology for the polygonalization of sparse circuit schematics	20021112 716/11
US 6457164 B1	Hetergeneous method for determining module placement in FPGAs	20020924 716/8
US 6366874 B1	System and method for browsing graphically an electronic design based on a hardware descripti	20020402 703/14
US 6360191 B1	Method and apparatus for automated design of complex structures using genetic programming	20020319 703/6
US 6353915 B1	Methods for evaluating systems of electronic components	20020305 716/4
US 6339836 B1	Automated design partitioning	20020115 716/5
US 6292925 B1	Context-sensitive self implementing modules	20010918 716/8
US 6260182 B1	Method for specifying routing in a logic module by direct module communication	20010710 716/12
US 6243851 B1	Heterogeneous method for determining module placement in FPGAs	20010605 716/10

US 6216259 B1	Configuration of programmable logic devices with routing core generators	20010410	716/17
US 6216258 B1	FPGA modules parameterized by expressions	20010410	716/17
US 6078736 A	Method of designing FPGAs for dynamically reconfigurable computing	20000620	716/16
US 5946478 A	Method for generating a secure macro element of a design for a programmable IC	19990831	716/17
US 5867397 A	Method and apparatus for automated design of complex structures using genetic programming	19990202	703/14
US 5857109 A	Programmable logic device for real time video processing	19990105	712/37
US 5603043 A	System for compiling algorithmic language source code for implementation in programmable har	19970211	712/1
US 5535342 A	Pld connector for module having configuration of either first PLD or second PLD and reconfigura	19960709	710/315
US 5497498 A	Video processing module using a second programmable logic device which reconfigures a first p	19960305	710/104
US 5197016 A	Integrated silicon-software compiler	19930323	716/8
US 5111413 A	Computer-aided engineering	19920505	703/14
US 4922432 A	Knowledge based method and apparatus for designing integrated circuits using functional specif	19900501	716/17
US 6353915 B	Interconnected electronic components system evaluating method e.g. for circuit board assemblie	20020305	

Interference checking

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EAST SEARCH

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L#	Hits	Search String	Databases
L1	1309	((Integrated or digital) near2 circuit$1) and netlist	US-PGPUB
L2	34	1 and (edit$3 with netlist$1)	US-PGPUB
L7	13	2 and (edit$3 with (HDL or "hardware description language"))	US-PGPUB
L8	31	1 and (edit$3.CLM.)	US-PGPUB
L9	4	8 and (HDL.CLM.)	US-PGPUB
L10	2	8 and ("hardware description language".CLM.)	US-PGPUB
L11	5	9 or 10	US-PGPUB
L12	16	8 and (netlist.CLM.)	US-PGPUB
L13	2	8 and (versions.CLM.)	US-PGPUB
L14	17	11 or 12 or 13	US-PGPUB

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Document Kind Codes	Title	Issue Date	Current OR	Abstract
US 20050278682 A1	Determining hardware parameters specified when configurable IP is synthesized	20051215	716/18	
US 20050125750 A1	System and method for three-dimensional visualization and postprocessing of a system model	20050609	716/4	
US 20050097493 A1	Gate reuse methodology for diffused cell-based IP blocks in platform-based silicon products	20050505	716/11	
US 20050076316 A1	Design-manufacturing interface via a unified model	20050407	716/4	
US 20050044514 A1	Method and platform for integrated physical verifications and manufacturing enhancements	20050224	716/5	
US 20050027502 A1	Line modeling tool	20050203	703/15	
US 20030233219 A1	Method and apparatus emulating read only memories with combinatorial logic networks, and n	20031218	703/14	
US 20030135832 A1	Method for creating a design verification test bench	20030717	716/5	
US 20030126565 A1	Method and system for a timing based logic entry	20030703	716/3	
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21 Life after CMOS: Imminent or Irrelevant?: Carbon nanotube field-effect transistors and logic circuits

R. Martel, V. Derycke, J. Appenzeller, S. Wind, Ph. Avouris

June 2002 **Proceedings of the 39th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(454.98 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present recent advances in the understanding of the properties of semiconducting single wall carbon nanotube and in the exploration of their use as field-effect transistors (FETs). Both electrons and holes can be injected in a nanotube transistor by either controlling the metal-nanotube Schottky barriers present at the contacts or simply by doping the bulk of the nanotube. These methods give complementary nanotube FETs that can be integrated together to make inter- and intra-na ...

Keywords: FET, SWNT, Schottky barrier, carbon nanotube, circuits, field-effect transistor, inverter, logic gate, nanoelectronics, semiconductor

22 An Interconnect-Aware Methodology for Analog and Mixed Signal Design, Based on High Bandwidth (Over 40 Ghz) On-Chip Transmission Line Approach

D. Goren, M. Zelikson, T. Galambos, R. Gordin, B. Livshitz, A. Amir, A. Sherman, I. Wagner

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Computer Society

Full text available: pdf(229.96 KB) Publisher Site Additional Information: full citation, abstract, citings

This paper presents an on-chip, interconnect-awaremethodology for high-speed analog and mixed signal(AMS) design which enables early incorporation of on-chiptransmission line (T-line) components into AMS design flow.The proposed solution is based on a set of parameterizedT-line structures, which include single and two coupled microstriplines with optional side shielding, accompanied bycompact true transient models. The models account for frequencydependent skin and proximity effects, while maint ...

23 From System Specification To Layout: Seamless Top-Down Design Methods for Analog and Mixed-Signal Applications

R. Sommer, I. Rugen-Herzig, E. Hennig, U. Gatti, P. Malcovati, F. Maloberti, K. Einwich, C.

Clauss, P. Schwarz, G. Noessing
March 2002 **Proceedings of the conference on Design, automation and test in Europe**
Publisher: IEEE Computer Society
Full text available: pdf(462.49 KB) Publisher Site
Additional Information: full citation, abstract, citings

Deisgn automation for analog/mixed-signal (A/MS) circuits and systems is still lagging behind compared to what has been reached in the digital area.As System-on-Chip (SoC) designs include analog components in more cases, these analog parts become even more a bottle neck in the overall design process.The paper is dedicated to latest R&D activities within the MEDEA+ project ANASTASIA+.Main focus will be the development of seamless top-down design methods for integrated analog and misx-signal syste ...

24 Internet-Based Collaborative Test Generation with MOSCITO
A. Schneider, K. Diener, E. Ivask, J. Raik, R. Ubar, P. Miklos, T. Cibáková, E. Gramatová
March 2002 **Proceedings of the conference on Design, automation and test in Europe**
Publisher: IEEE Computer Society
Full text available: pdf(419.63 KB) Publisher Site
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This paper offers an Internet-based environment forenhancing problem-specific design flows with test patterngeneration and fault simulation capabilities. AutomaticTest Pattern Generation (ATPG) and fault simulation toolsat structural and hierarchical levels available at geographicallydifferent places running under the virtual environmentusing the MOSCITO system are presented. Thesetools can be used separately, or in multiple applications,for test pattern generation of digital circuits. In order ...

25 Architecture Analysis and Automation: Automatic layout of domain-specific reconfigurable subsystems for system-on-a-chip
Shawn Phillips, Scott Hauck
February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(751.48 KB)
Additional Information: full citation, abstract, references, citings, index terms

When designing SOCs, a unique opportunity exists to generate custom FPGA architectures that are specific to the application domain in which the device will be used. The inclusion of such a device will provide an efficient compromise between the flexibility of software and the performance of hardware, while at the same time allowing for post-fabrication modification of circuits. To automate the layout of reconfigurable subsystems for system-on -a-chip we present template reduction, standard cell, ...

Keywords: automatic layout generation, domain-specific FPGA, standard cells, system-on a-chip

26 NanoFabrics: spatial computing using molecular electronics
Seth Copen Goldstein, Mihai Budiu
May 2001 **ACM SIGARCH Computer Architecture News , Proceedings of the 28th annual international symposium on Computer architecture ISCA '01**, Volume 29 Issue 2
Publisher: ACM Press
Full text available: pdf(996.26 KB)
Additional Information: full citation, abstract, references, citings, index terms

The continuation of the remarkable exponential increases in processing power over the

recent past faces imminent challenges due in part to the physics of deep-submicron CMOS devices and the costs of both chip masks and future fabrication plants. A promising solution to these problems is offered by an alternative to CMOS-based computing, chemically assembled electronic nanotechnology (CAEN).

In this paper we outline how CAEN-based computing can become a reality. We briefly describe rec ...

27 On rent's rule for rectangular regions

J. Dambre, P. Verplaetse, D. Stroobandt, J. Van Campenhout

March 2001 **Proceedings of the 2001 international workshop on System-level interconnect prediction**

Publisher: ACM Press

Full text available: pdf(272.25 KB) Additional Information: full citation, abstract, references, citings, index terms

A priori wirelength estimates are based on a terminal-gate relationship known as Rent's rule. Conventional models apply Rent's rule in 2D on square or diamond-shaped regions. However, more advanced applications of wirelength estimation require the use of Rent's rule on layout regions with different shapes. In this paper, we systematically study the layout Rent parameters of rectangular regions in a 2D layout medium. For this purpose, we derive a theoretical model for the pin versus gate rel ...

Keywords: Rent's rule, layout Rent parameters, rectangular layout region, wirelength distribution

28 Wiring requirement and three-dimensional integration of field-programmable gate arrays

Arifur Rahman, Shamik Das, Anantha Chandraksan, Rafael Reif

March 2001 **Proceedings of the 2001 international workshop on System-level interconnect prediction**

Publisher: ACM Press

Full text available: pdf(117.63 KB) Additional Information: full citation, abstract, references, index terms

In this paper analytical models for predicting interconnect requireðments in field-programmable gate arrays (FPGAs) are presented, and opportunities for 3-D implementation of FPGAs are examined. The analytical models for 2-D FPGAs are calibrated by routing and placement experiments with benchmark circuits and extended to 3-D FPGAs. Based on system-level modeling, we find that in FPGAs with 20K 4-input look-up tables, the reduction in channel width, interconnect delay, and power dissipation ...

Keywords: 3-D integrated circuits, FPGA, system-level modeling, wire-length

29 Run-Time defect tolerance using JBits

Prasanna Sundararajan, Steven A. Guccione

February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(135.45 KB) Additional Information: full citation, abstract, references, citings, index terms

The ability to tolerate defects in semiconductor devices has the potential for both increasing yields of devices being manufactured and making it economically feasible to manufacture even larger devices. While FPGA devices appear to be well suited to providing defect tolerance, practical application of existing research and techniques has

been somewhat elusive. One barrier to acceptance is that existing defect tolerance techniques for FPGAs have tended to rely on either modifications to de ...

Keywords: FPGA, Java, cores, defect tolerance, run-time reconfiguration

30 System level design research in an industrial setting (invited talks): YAML: a tool for hardware design visualization and capture

Vivek Sinha, Frederic Doucet, Chuck Siska, Rajesh Gupta, Stan Liao, Abhijit Ghosh
September 2000 **Proceedings of the 13th international symposium on System synthesis**
Publisher: IEEE Computer Society
Full text available: pdf(114.62 KB) Additional Information: full citation, abstract, references

Design visualization is an important part of the system design process. In practice, systems are often visualized using a combination of structural and functional entities. In this paper, we describe an approach that helps to capture the structural aspects of a design at a high level of abstraction and enables the system designer to enter designs "schematically" using predefined structural and functional entities conforming to UML notation. The corresponding tool, YAML (Yet Another UML front end ...

31 A current driven routing and verification methodology for analog applications

Thorsten Adler, Hiltrud Brocke, Lars Hedrich, Erich Barke
June 2000 **Proceedings of the 37th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(182.57 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a new methodology for current driven routing and layout verification for analog applications used to avoid defects due to electromigration. The methodology presented uses a commercial simulator to calculate the current flow at all terminals of the analog circuit. Afterwards maximum currents per terminal are extracted and used as guidance for the Current Driven Router (CDR) which is capable of routing analog multiterminal signal nets with current driven wire widths.
Keywords: Steiner tree, current density, design methodology, electromigration, multiterminal signal nets, routing, verification

32 Designing systems-on-chip using cores

Reinaldo A. Bergamaschi, William R. Lee
June 2000 **Proceedings of the 37th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(88.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Leading-edge systems-on-chip (SoC) being designed today could reach 20 Million gates and 0.5 to 1 GHz operating frequency. In order to implement such systems, designers are increasingly relying on reuse of Intellectual property (IP) blocks. Since IP blocks are pre-designed and pre-verified, the designer can concentrate on the complete system without having to worry about the correctness or performance of the individual components. That is the goal, in theory. In practice, assembling on SoC ...

33 Guidelines for using multiple views in information visualization

Michelle Q. Wang Baldonado, Allison Woodruff, Allan Kuchinsky
May 2000 **Proceedings of the working conference on Advanced visual interfaces**
Publisher: ACM Press

Full text available: pdf(2.13 MB) Additional Information: full citation, abstract, references, citings, index terms

A multiple view system uses two or more distinct views to support the investigation of a single conceptual entity. Many such systems exist, ranging from computer-aided design (CAD) systems for chip design that display both the logical structure and the actual geometry of the integrated circuit to overview-plus-detail systems that show both an overview for context and a zoomed-in-view for detail. Designers of these systems must make a variety of design decisions, ranging from determining lay ...

Keywords: design guidelines, information visualization, multiple views, usability heuristics, user interfaces

34 Layout tools for analog ICs and mixed-signal SoCs: a survey

Rob A. Rutenbar, John M. Cohn
May 2000 **Proceedings of the 2000 international symposium on Physical design**
Publisher: ACM Press
Full text available: pdf(247.03 KB) Additional Information: full citation, references

35 Graphical user interface of FIESTA—software for faults identification and estimation of testability of VLSI circuits

Mykola Blyzniuk, Taras Panchak, Wieslaw Kuzmicz, Witold Pleskacz
February 2000 **Proceedings of the symposium on Contemporary computing in Ukraine**
Publisher: ACM Press
Full text available: pdf(7.00 MB) Additional Information: full citation, abstract, index terms

We present the graphical user interface (GUI) of FIESTA software tools. It is based on the proposed principles of open systems development. FIESTA was designed as UNIX application and works under Solaris 2.5.1. Graphical user interface of FIESTA has been developed with the use of Tel/Tk 8.2 design environment.

Keywords: faults identification, graphical user interface, software tools, usefulness of test vector components

36 CMAPS: a cosynthesis methodology for application-oriented parallel systems

Pao-Ann Hsiung
January 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 1
Publisher: ACM Press
Full text available: pdf(209.29 KB) Additional Information: full citation, abstract, references, citings, index terms

Currently, a lot of research is devoted to system design, and little work is done on requirements analysis. Besides going from specification to design, one of our main objectives is to show how an application problem can be transformed into specifications. Working from the hardware-software codesign perspective, a system is designed starting from an application problem itself, rather than the detailed behavioral specifications. Given an application problem ...

Keywords: application-oriented general-purpose multiprocessors, hardware-software modeling and cosynthesis, requirements analysis

37 Operational simulation of an x-ray lithography cell: comparison of 200mm and 300mm wafers
K. Preston White, Walter J. Trybula
December 1999 **Proceedings of the 31st conference on Winter simulation: Simulation--a bridge to the future - Volume 1**
Publisher: ACM Press
Full text available: pdf(138.94 KB) Additional Information: full citation, references, index terms

38 Quo Vadis evolvable hardware?
Moshe Sipper, Daniel Mange, Eduardo Sanchez
April 1999 **Communications of the ACM**, Volume 42 Issue 4
Publisher: ACM Press
Full text available: pdf(409.06 KB) html(34.33 KB) Additional Information: full citation, references, citings, index terms

39 Re-configurable computing
Richard Swan, Anthony Wyatt, Richard Cant, Caroline Langensiepen
April 1999 **Crossroads**
Publisher: ACM Press
Full text available: html(43.04 KB) Additional Information: full citation, index terms

40 Field-programmable gate arrays
Pierre Marchal
April 1999 **Communications of the ACM**, Volume 42 Issue 4
Publisher: ACM Press
Full text available: pdf(161.87 KB) html(13.25 KB) Additional Information: full citation, references, index terms

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Relevance scale

1 Optimized Generation of Data-Path from C Codes for FPGAs
Zhi Guo, Betul Buyukkurt, Walid Najjar, Kees Vissers
March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1**
Publisher: IEEE Computer Society
Full text available: pdf(281.78 KB) Additional Information: full citation, abstract

FPGAs, as computing devices, offer significant speedup over microprocessors. Furthermore, their configurability offers an advantage over traditional ASICs. However, they do not yet enjoy high-level language programmability, as microprocessors do. This has become the main obstacle for their wider acceptance by application designers. ROCCC is a compiler designed to generate circuits from C source code to execute on FPGAs, more specifically on CSoCs. It generates RTL level HDLs from frequently exec ...

2 Hardware Accelerated Power Estimation
Joel Coburn, Srivaths Ravi, Anand Raghunathan
March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1**
Publisher: IEEE Computer Society
Full text available: pdf(193.63 KB) Additional Information: full citation, abstract

In this paper, we present power emulation, a novel design paradigm that utilizes hardware acceleration for the purpose of fast power estimation. Power emulation is based on the observation that the functions necessary for power estimation (power model evaluation, aggregation, etc.) can be implemented as hardware circuits. Therefore, we can enhance any given design with "power estimation hardware", map it to a prototyping platform, and exercise it with any given test stimuli to obtain power consu ...

3 Computation algorithms for FPGA: Floating-point sparse matrix-vector multiply for FPGAs
Michael deLorimier, André DeHon
February 2005 **Proceedings of the 2005 ACM/SIGDA 13th international symposium on Field-programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(344.21 KB) Additional Information: full citation, abstract, references, index terms

Large, high density FPGAs with high local distributed memory bandwidth surpass the peak floating-point performance of high-end, general-purpose processors. Microprocessors do not deliver near their peak floating-point performance on efficient algorithms that use the

Sparse Matrix-Vector Multiply (SMVM) kernel. In fact, it is not uncommon for microprocessors to yield only 10--20% of their peak floating-point performance when computing SMVM. We develop and analyze a scalable SMVM implementation on ...

Keywords: FPGA, compressed sparse row, floating point, reconfigurable architecture, sparse matrix

4 Verification: Separation of concerns: overhead in modeling and efficient simulation techniques

Guang Yang, Alberto Sangiovanni-Vincentelli, Yosinori Watanabe, Felice Balarin

September 2004 **Proceedings of the 4th ACM international conference on Embedded software EMSOFT '04**

Publisher: ACM Press

Full text available: pdf(208.12 KB) Additional Information: full citation, abstract, references, index terms

Separating the description of important aspects of a design such as behavior and architecture, or computation and communication, may yield significant advantages in design time as well as in re-usability of the design. However, exploiting fully the re-usability opportunities offered by this approach implies to keep the various aspects of the design separated while verifying the design at a given level of abstraction. In particular, simulation of the design may undergo significant overhead versus ...

Keywords: interleaving concurrency, orthogonalization of conerns, platform-based design, simulation

5 Application specific processors: A low power architecture for embedded perception

Binu Mathew, Al Davis, Mike Parker

September 2004 **Proceedings of the 2004 international conference on Compilers, architecture, and synthesis for embedded systems**

Publisher: ACM Press

Full text available: pdf(310.49 KB) Additional Information: full citation, abstract, references, index terms

Recognizing speech, gestures, and visual features are important interface capabilities for future embedded mobile systems. Unfortunately, the real-time performance requirements of complex perception applications cannot be met by current embedded processors and often even exceed the performance of high performance microprocessors whose energy consumption far exceeds embedded energy budgets. Though custom ASICs provide a solution to this problem, they incur expensive and lengthy design cycles and ...

Keywords: VLIW, computer vision, embedded systems, low power design, perception, speech recognition, stream processor

6 Practical issues in logic synthesis: Enhancing the performance of multi-cycle path analysis in an industrial setting

Hiroyuki Higuchi, Yusuke Matsunaga

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**

Publisher: IEEE Press , IEEE Press

Full text available: pdf(117.87 KB) Publisher Site Additional Information: full citation, abstract, references

In this paper we enhance the performance of multi-cycle path analysis in an industrial

setting. Industrial designs are, in general, more complicated, but contain more information than fundamental sequential circuits. We show how such information is used for improving the quality and the efficiency of multi-cycle path analysis. Specifically, we propose local FSM learning to take into account reachability information. We also propose **FF** enable learning to accelerate multi-cycle path analysi ...

7 (Special session) embedded tutorial: RF modeling and design methodology: RF design methodologies bridging system-IC-module design

Robert A. Mullen

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**

Publisher: IEEE Press , IEEE Press

Full text available: pdf(538.14 KB) Publisher Site Additional Information: full citation, abstract, references

There has been a long-standing need to link the RF design domains into a connected, common design environment. Such a methodology is possible through implementing system-level behavioral models with different levels of abstraction that can be modeled or co-simulated at the IC circuit level. At module or board design, it is possible to link and simulate multiple chips with board-level components and parastics in an RFIC design environment.With today's more complex IC designs that are heading towa ...

8 (Special session) invited talks: c-based design examples: Using C based logic synthesis to bridge the productivity gap

Chris Sullivan, Alex Wilson, Stephen Chappell

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**

Publisher: IEEE Press , IEEE Press

Full text available: pdf(375.82 KB) Publisher Site Additional Information: full citation, abstract

Digital circuits from software designs and formal executable specifications can be automatically synthesized using hardware compilation or 'C based logic synthesis'. Designs can be verified using that same formal specification and coupled with the increasing deployment of higher-level C based languages and IP reuse in hardware design and system codesign, C based logic synthesis is enabling new methodologies and levels of designer productivity. In this paper we discuss the rationale for such a sy ...

9 Testbench, verification and debugging: practical considerations: Behavioral consistency of C and verilog programs using bounded model checking

Edmund Clarke, Daniel Kroening, Karen Yorav

June 2003 **Proceedings of the 40th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(142.69 KB) Additional Information: full citation, references, citings, index terms

Keywords: ANSI-C, equivalence checking, verilog

10 VLSI design: Zero overhead watermarking technique for FPGA designs

Adarsh K. Jain, Lin Yuan, Pushkin R. Pari, Gang Qu
April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI**
Publisher: ACM Press
Full text available: pdf(327.86 KB) Additional Information: full citation, abstract, references, index terms

FPGAs, because of their re-programmability, are becoming very popular for creating and exchanging VLSI intellectual properties (IPs) in the reuse-based design paradigm. Existing watermarking and fingerprinting techniques successfully embed identification information into FPGA designs to deter IP infringement. However, such methods incur timing and/or resource overhead, unpredictable at times, which causes performance degradation. In this paper, we propose a new FPGA watermarking technique that g ...

Keywords: FPGA, IP protection, configuration bitstream, performance, place and route, timing analyzer, user constraint file, zero overhead

11 Hardware/Software Design Space Exploration for a Reconfigurable Processor
Alberto La Rosa, Luciano Lavagno, Claudio Passerone
March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**
Publisher: IEEE Computer Society
Full text available: pdf(103.11 KB) Publisher Site Additional Information: full citation, abstract, index terms

This paper describes an approach to hardware/software design space exploration for reconfigurable processors. The existing compiler tool-chain, because of the user-definable instructions, needs to be extended in order to offer developers an easy way to explore design space. Such extension often is not easy to use for developer that have only a software background, thus ignoring reconfigurable architecture details or hardware logic synthesis on FPGA. Our approach differs from others because it is ...

12 *Quick piping*: a fast, high-level model for describing processor pipelines
Christopher W. Milner, Jack W. Davidson
June 2002 **ACM SIGPLAN Notices , Proceedings of the joint conference on Languages, compilers and tools for embedded systems: software and compilers for embedded systems LCTES/SCOPES '02**, Volume 37 Issue 7
Publisher: ACM Press
Full text available: pdf(206.06 KB) Additional Information: full citation, abstract, references, index terms

Responding to marketplace needs, today's embedded processors must feature a flexible core that allows easy modification with fast time to market. In this environment, embedded processors are increasingly reliant on flexible support tools. This paper presents one such tool, called *Quick Piping*, a new, high-level formalism for modeling processor pipelines. *Quick Piping* consists of three primary components that together provide an easy-to-build, reusable processor description:

Keywords: embedded systems, modeling of computer architecture, pipelines

13 Advances in synthesis: Implementing asynchronous circuits using a conventional EDA tool-flow
Christos P. Sotiriou
June 2002 **Proceedings of the 39th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(107.01 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents an approach by which asynchronous circuits can be realised with a conventional EDA tool flow and conventional standard cell libraries. Based on a gate-level asynchronous circuit implementation technique, direct-mapping, and by identifying the delay constraints and exploiting certain EDA tool features, this paper demonstrates that a conventional EDA tool flow can be used to describe, place, route and timing-verify asynchronous circuits.

Keywords: EDA, asynchronous, tool-flow

14 Generalized Early Evaluation in Self-Timed Circuits

M. Thornton, K. Fazel, R. Reese, C. Traver

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Computer Society

Full text available: pdf(118.09 KB) Publisher Site

Additional Information: full citation, abstract

Phased logic has been proposed as a technique for realizingself-timed circuitry that is delay-insensitive and requiresno global clock signals. Early evaluation techniqueshave been applied to asynchronous circuits in the past inorder to achieve throughput increases. A general methodfor computing early evaluation functions is presented forthis design style. Experimental results are given that showthe increase in throughput of various benchmark circuits.The results show that as much as a 30% speedu ...

15 From System Specification To Layout: Seamless Top-Down Design Methods for Analog and Mixed-Signal Applications

R. Sommer, I. Rugen-Herzig, E. Hennig, U. Gatti, P. Malcovati, F. Maloberti, K. Einwich, C. Clauss, P. Schwarz, G. Noessing

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Computer Society

Full text available: pdf(462.49 KB) Publisher Site

Additional Information: full citation, abstract, citings

Deisgn automation for analog/mixed-signal (A/MS) circuits and systems is still lagging behind compared to what has been reached in the digital area.As System-on-Chip (SoC) designs include analog components in more cases, these analog parts become even more a bottle neck in the overall design process.The paper is dedicated to latest R&D activities within the MEDEA+ project ANASTASIA+.Main focus will be the development of seamless top-down design methods for integrated analog and misx-signal syste ...

16 Run-Time defect tolerance using JBits

Prasanna Sundararajan, Steven A. Guccione

February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(135.45 KB)

Additional Information: full citation, abstract, references, citings, index terms

The ability to tolerate defects in semiconductor devices has the potential for both increasing yields of devices being manufactured and making it economically feasible to manufacture even larger devices. While FPGA devices appear to be well suited to providing defect tolerance, practical application of existing research and techniques has been somewhat elusive. One barrier to acceptance is that existing defect tolerance techniques for FPGAs have tended to rely on either modifications to de ...

Keywords: FPGA, Java, cores, defect tolerance, run-time reconfiguration

17 System level design research in an industrial setting (invited talks): YAML: a tool for hardware design visualization and capture

Vivek Sinha, Frederic Doucet, Chuck Siska, Rajesh Gupta, Stan Liao, Abhijit Ghosh

September 2000 **Proceedings of the 13th international symposium on System synthesis**

Publisher: IEEE Computer Society

Full text available: pdf(114.62 KB) Additional Information: full citation, abstract, references

Design visualization is an important part of the system design process. In practice, systems are often visualized using a combination of structural and functional entities. In this paper, we describe an approach that helps to capture the structural aspects of a design at a high level of abstraction and enables the system designer to enter designs "schematically" using predefined structural and functional entities conforming to UML notation. The corresponding tool, YAML (Yet Another UML front end ...

18 System level design research in an industrial setting (invited talks): IP reuse in the system on a chip era

Warren Savage, John Chilton, Raul Camposano

September 2000 **Proceedings of the 13th international symposium on System synthesis**

Publisher: IEEE Computer Society

Full text available: pdf(728.70 KB) Additional Information: full citation, abstract, references

Intellectual Property (IP) Reuse is one of the keys for System on a Chip (SoC) design productivity improvement. Although IP reuse has been explored both technically and as a business for many years, only recently systematic approaches based on EDA technology are starting to emerge in the marketplace. This paper gives an introduction to IP creation, IP conversion and the necessary infrastructure. We address the technical challenges and show that a strict quality based design methodology is the co ...

19 Efficient building block based RTL code generation from synchronous data flow graphs

Jens Horstmannshoff, Heinrich Meyr

June 2000 **Proceedings of the 37th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(86.17 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a RTL-HDL code generation from synchronous data-flow graphs which supports the building block based design of data-flow oriented ASIC systems. Here, additional interfacing and controlling hardware is generated to adapt non-matching interfacing properties. In order to reduce interface register cost, a retiming approach is taken to schedule optimum building block activation times. The code generation methodology is compared to an existing approach using different case stud ...

20 Modeling design constraints and biasing in simulation using BDDs

Jun Yuan, Kurt Shultz, Carl Pixley, Hillel Miller, Adnan Aziz

November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Press

Full text available: pdf(133.50 KB) Additional Information: full citation, abstract, references, citings, index terms

Constraining and input biasing are frequently used techniques in functional verification methodologies based on randomized simulation generation. Constraints confine the simulation to a legal input space, while input biasing, which can be considered as a

probabilistic constraint, makes it easier to cover interesting "corner" cases. In this paper, we propose to use constraints and biasing to form a simulation environment instead of using an expli ...

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21 Optimized System Synthesis of Complex RT Level Building Blocks from Multirate Dataflow Graphs

Jens Horstmannshoff, Heinrich Meyr
November 1999 **Proceedings of the 12th international symposium on System synthesis**
Publisher: IEEE Computer Society
Full text available: pdf(160.15 KB) Publisher Site
Additional Information: full citation, abstract, citings

In order to cope with the ever increasing complexity of todays application specific integrated circuits, a building block based design methodology is established. The system is composed of high level building blocks of which some are reused from previous designs while others might have been created by behavioral synthesis. In data flow oriented designs, these blocks usually have complex non-matching interface properties, making it necessary to generate additional interfacing and controlling hard ...

22 Robust techniques for watermarking sequential circuit designs

Arlindo L. Oliveira
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(145.39 KB) Additional Information: full citation, references, citings, index terms

23 A practical approach to multiple-class retiming

Klaus Eckl, Jean Christophe Madre, Peter Zepter, Christian Legl
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(106.37 KB) Additional Information: full citation, references, citings, index terms

24 Robust FPGA intellectual property protection through multiple small watermarks

John Lach, William H. Mangione-Smith, Miodrag Potkonjak
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(119.08 KB) Additional Information: full citation, references, citings, index terms

Keywords: field programmable gate array (FPGA), intellectual property protection, watermarking

25 SIGda '96, workshop: how do we expedite the commercial use of Ada?

Robert C. Leif
March 1999 **ACM SIGAda Ada Letters**, Volume XIX Issue 1
Publisher: ACM Press
Full text available: pdf(858.93 KB) Additional Information: full citation, citings, index terms

26 Flexible design of SPARC cores: a quantitative study

Tomás Bautista, Antonio Núñez
March 1999 **Proceedings of the seventh international workshop on Hardware/software codesign**
Publisher: ACM Press
Full text available: pdf(468.40 KB) Additional Information: full citation, references, index terms

27 Practical experiences with standard-cell based datapath design tools: do we really need regular layouts?

Paolo Ienne, Alexander Grießing
May 1998 **Proceedings of the 35th annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(263.99 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Commercial tools for standard-cell based datapath design are here classed according to design flows, and the advantages of each class are discussed with the results of two test circuits. Algorithmic generation of netlists and of relative cell placement can help reducing area but, contrary to common belief, appears often detrimental to speed. Extraction of regularity from synthesized netlists is difficult and requires counterproductive simplifications to the synthesis process. Most p ...

Keywords: custom sizing, migration, timing optimazation

28 Design of a SPDIF receiver using protocol compiler

Ulrich Holtmann, Peter Blinzer
May 1998 **Proceedings of the 35th annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(348.72 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

This paper describes the design of a receiver for the digital audio signal SPDIF used by CD-ROM players. The design was done with Protocol Compiler, a high-level synthesis tool for the design of structured data stream processing controllers. Compared to traditional RTL design, Protocol Compiler makes entry, debugging, and re-use easier. Design time was cut by factor 2 while the results in terms of area and delay are competitive.

Keywords: high-level synthesis, telecommunication

29 Design of future systems

I. Page

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Computer Society

Full text available: pdf(142.27 KB) Publisher Site

Additional Information: full citation, abstract, references, index terms

This paper describes a vision in which future systems consisting of novel hardware and software components are designed and implemented by a single type of professional engineer. That professional has more in common with today's programmer than a hardware designer, although both of these existing bodies of professionals have a strong contribution to make to understanding, defining and bringing about this transformation in product creation.

Keywords: FPGA, hardware compilation, hardware synthesis, parallel programming

30 Innovative system-level design environment based on FORM for transport processing system

K. Higuchi, K. Shirakawa

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Computer Society

Full text available: pdf(115.71 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

This paper presents a system-level design environment for data transport processing systems. In this environment, designers can easily verify system behavior by formally defining data structures and their related actions, without considering detailed timing. In addition, the verified specification can be translated into synthesizable RTL descriptions by a dedicated RTL generator. Thus, using lower-level EDA tools, actual hardware can be obtained directly from a system-level specification.

Keywords: Formal specification, System design, Transport processing system, RTL generation, Specification editor, System level simulation

31 A real-time RTL engineering-change method supporting on-line debugging for logic-emulation applications

Wen-Jong Fang, Allen C.-H. Wu, Ti-Yen Yen

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Publisher: ACM Press

Full text available: pdf(236.13 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

In recent years, logic emulation has been widely usedas a key design verification methodology in many complex CPU, telecom, and multimedia design projects. When using logic emulation for design verification, designers often need toperform engineering changes as a result of design debugging of a design specificationmodification. One of the essential issues to engineeringchanges is the turn-around time. Ideally, after designers modify their designs, they resume their debugging and verification tas ...

32 CAD and foundries for microsystems

J. M. Karam, B. Courtois, H. Boutamine, P. Drake, A. Poppe, V. Szekely, M. Rencz, K. Hofmann, M. Glesner

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Publisher: ACM Press

Full text available: pdf(304.07 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

Besides foundry facilities, Computer-Aided Design (CAD)tools are also required to move microsystems from researchprototypes to an industrial market. Currently available CADtools need extensions before they can be used for theautomated design of micromachined devices.This paper presents a low cost access to microsystemtechnology (MST), applied by the CMP service, and based onthe use of existing microelectronics production lines, withadditional post-processing for microsystem specific 2D and3D str ...

33 Synthesis of multi-rate and variable rate circuits for high speed telecommunications applications

P. Schaumont, S. Vernalde, L. Rijnders, M. Engels, I. Bolsens

March 1997 **Proceedings of the 1997 European conference on Design and Test**

Publisher: IEEE Computer Society

Full text available: pdf(568.53 KB) Publisher Site

Additional Information: full citation, abstract, citings

A design methodology for the synthesis of digital circuits used in high throughput digital modems is presented. The methodology spans digital modern design from the link level to the gate level. The methodology uses a C++-based untimed dataflow system description, which is gradually refined to an optimized, bit-true and clock cycle true C++-description. Through this refinement, a bridge from link level design semantics to architectural VHDL semantics is made within one and the same environment.

Keywords: C++-based untimed dataflow system, VHDL semantics, clock cycle true C++-description, design methodology, design semantics, digital circuit synthesis, digital integrated circuits, digital modems, gate level, link level, multi-rate circuits, variable rate circuits

34 An observability-based code coverage metric for functional simulation

Srinivas Devadas, Abhijit Ghosh, Kurt Keutzer

January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society

Full text available: pdf(124.26 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

Functional simulation is the most widely used method for design verification. At various levels of abstraction, e.g., behavioral, register-transfer level and gate level, the designer simulates the design using a large number of vectors attempting to debug and verify the design. A major problem with functional simulation is the lack of good metrics and tools to evaluate the quality of a set of functional vectors. Metrics used currently are based on instruction counts and are quite simplistic. Des ...

Keywords: verification, functional simulation, code coverage

35 A top down mixed-signal design methodology using a mixed-signal simulator and

analog HDL
T. Murayama, Y. Gendai
September 1996 **Proceedings of the conference on European design automation**
Publisher: IEEE Computer Society
Full text available: pdf(273.54 KB) Additional Information: full citation, references, index terms

36 Combined control flow dominated and data flow dominated high-level synthesis
E. Berrebi, P. Kission, S. Vernalde, S. De Troch, J. C. Herluison, J. Fréhel, A. A. Jerraya, I. Bolsens
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(194.86 KB) Additional Information: full citation, references, citings, index terms

37 Structured design implementation: a strategy for implementing regular datapaths on FPGAs
Andreas Koch
February 1996 **Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(328.84 KB) Additional Information: full citation, references, citings, index terms

38 Automatic generation of functional vectors using the extended finite state machine model
Kwang-Ting Cheng, A. S. Krishnakumar
January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1
Publisher: ACM Press
Full text available: pdf(455.35 KB) Additional Information: full citation, abstract, references, citings, index terms, review

We present a method of automatic generation of functional vectors for sequential circuits. These vectors can be used for design verification, manufacturing testing, or power estimation. A high-level description of the circuit in VHDL or C is assumed available. Our method automatically transforms the high-level description of a circuit in VHDL or C into an extended finite state machine (EFSM) model that is used to generate functional vectors. The EFSM model is a generalization of the traditi ...

Keywords: automatic test generation, design verification, extended finite state machines, functional testing

39 Controlling change propagation and project policies in IC design
Y. Mathys, M. Morgan, S. Soudagar
March 1995 **Proceedings of the 1995 European conference on Design and Test**
Publisher: IEEE Computer Society
Full text available: pdf(645.11 KB) Publisher Site Additional Information: full citation, abstract

Today's large IC designs involve highly partitioned, highly coupled and voluminous design data evolving over time. Tracking design state is becoming an essential component of

design tracking systems. In this paper we present the project BluePrint, a design data flow management tool which is an extension to the DAMOCLES tracking system. The project BluePrint is event driven. It defines project data dependencies and controls change propagation. The BluePrint allows the separation of project specif ...

Keywords: BluePrint, IC design, change propagation, circuit CAD, data flow analysis, data flow management tool, design data, design state, design tracking systems, discrete event simulation, event driven, integrated circuit design, project data dependencies, project engineering, project policies, tool integration

40 Input and output processor for an ATM high speed switch (2.5 Gb/s): the CMC



P. Plaza, J. C. Diaz, F. Calvo, L. Merayo, M. Zamboni, P. Scarfone, M. Barbini

March 1995 **Proceedings of the 1995 European conference on Design and Test**

Publisher: IEEE Computer Society

Full text available: pdf(574.66 KB) Publisher Site

Additional Information: full citation, abstract

The design and implementation of an input/output processor for an ATM switch are described. This IC was realized on a 0.7 /spl mu/m BiCMOS technology. To manipulate ATM cells at a frequency of 311 MHz (STM16) at the I/O of the chip, ECL blocks were employed. The core of the chip is composed of CMOS cells that run at a maximum clock speed of 65 MHz. Pure analog blocks were not needed. The CMC is capable of functioning in two different modes: 1. The CM mode, in which 8 bit wide ATM cells are conve ...

Keywords: 0.7 micron, 2.5 Gbit/s, 311 MHz, 65 MHz, 8.2 W, ATM high speed switch, BiCMOS digital integrated circuits, BiCMOS technology, CMC, CPGA-319 pin package, DSP chip, ECL blocks, STM16, asynchronous transfer mode, custom parallel format, digital signal processing chips, electronic switching systems, emitter-coupled logic, input/output processor

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41 From System Specification To Layout: Seamless Top-Down Design Methods for Analog and Mixed-Signal Applications

R. Sommer, I. Rugen-Herzig, E. Hennig, U. Gatti, P. Malcovati, F. Maloberti, K. Einwich, C. Clauss, P. Schwarz, G. Noessing

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Computer Society

Full text available: pdf(462.49 KB) Publisher Site

Additional Information: full citation, abstract, citings

Deisgn automation for analog/mixed-signal (A/MS) circuits and systems is still lagging behind compared to what has been reached in the digital area.As System-on-Chip (SoC) designs include analog components in more cases, these analog parts become even more a bottle neck in the overall design process.The paper is dedicated to latest R&D activities within the MEDEA+ project ANASTASIA+.Main focus will be the development of seamless top-down design methods for integrated analog and misx-signal syste ...

42 Automated Modeling of Custom Digital Circuits for Test

S. Bose

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Computer Society

Full text available: pdf(156.90 KB) Publisher Site

Additional Information: full citation, abstract

Models meant for logic verification and simulation areoften used for ATPG. For custom digital circuits, these modelscontain many tristate devices, which leads to lower faultcoverage. Unlike other research in the literature, the modelingalgorithms presented in this paper analyze each channelconnected component in the context of its environment,thereby capturing the relationship among its input signals.This reduces the number of tristates and increases the modelingefficiency, as measured by fault ...

43 Architecture Analysis and Automation: Automatic layout of domain-specific reconfigurable subsystems for system-on-a-chip

Shawn Phillips, Scott Hauck

February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**

Publisher: ACM Press

Additional Information: full citation, abstract, references, citings, index

Full text available: pdf(751.48 KB) terms

When designing SOCs, a unique opportunity exists to generate custom FPGA architectures that are specific to the application domain in which the device will be used. The inclusion of such a device will provide an efficient compromise between the flexibility of software and the performance of hardware, while at the same time allowing for post-fabrication modification of circuits. To automate the layout of reconfigurable subsystems for system-on -a-chip we present template reduction, standard cell, ...

Keywords: automatic layout generation, domain-specific FPGA, standard cells, system-on a-chip

44 Synthesis, Verification and Test: Timing verification of dynamically reconfigurable logic for the xilinx virtex FPGA series

Ian Robertson, James Irvine, Patrick Lysaght, David Robinson
February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(610.49 KB) Additional Information: full citation, abstract, references, citings

This paper reports on a method for extending existing VHDL design and verification software available for the Xilinx Virtex series of FPGAs. It allows the designer to apply standard hardware design and verification tools to the design of dynamically reconfigurable logic (DRL). The technique involves the conversion of a dynamic design into multiple static designs, suitable for input to standard synthesis and APR tools. For timing and functional verification after APR, the sections of the design c ...

Keywords: FPGA, dynamic reconfiguration, run-time reconfiguration, verification

45 Physical Design: EVE: a CAD tool for manual placement and pipelining assistance of FPGA circuits

William Chow, Jonathan Rose
February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(352.87 KB) Additional Information: full citation, abstract, references, citings

As FPGAs push ever deeper into mainstream digital design, there is an increasing desire for high-performance circuits. This paper describes a manual editor, called EVE, which can assist a designer to perform manual packing, placement and pipelining of commercial FPGA circuits to achieve a meaningful increase in performance. This effort is inspired by Von Herzen's paper [15] [16], which proposed the notion of an "Event Horizon" - a high-speed circuit design approach in which complete knowledge of ...

Keywords: FPGA, event horizon, manual placement and pipelining, programmable logic

46 Parallel dedicated hardware devices for heterogeneous computations

Alessandro Marongiu, Paolo Palazzari, Vittorio Rosato
November 2001 **Proceedings of the 2001 ACM/IEEE conference on Supercomputing (CDROM)**
Publisher: ACM Press
Full text available: pdf(234.51 KB) Additional Information: full citation, abstract, references, index terms

We describe a design methodology which allows a fast design and prototyping of

dedicated hardware devices to be used in *heterogeneous* computations. The platforms used in heterogeneous computations consist of a general-purpose COTS architecture which hosts a dedicated hardware device; parts of the computation are mapped onto the former, parts onto the latter, in a way to improve the overall computation efficiency. We report the design and the prototyping of a FPGA-based hardware board to b ...

Keywords: dedicated hardware device, low-autocorrelation binary sequences, systems of affine recurrence equations

47 Learning evaluation functions to improve optimization by local search

Justin Boyan, Andrew W. Moore
September 2001 **The Journal of Machine Learning Research**, Volume 1
Publisher: MIT Press
Full text available: pdf(643.21 KB) Additional Information: full citation, abstract, citings

This paper describes algorithms that learn to improve search performance on large-scale optimization tasks. The main algorithm, STAGE, works by learning an evaluation function that predicts the outcome of a local search algorithm, such as hillclimbing or Walksat, from features of states visited during search. The learned evaluation function is then used to bias future search trajectories toward better optima on the same problem. Another algorithm, X-STAGE, transfers previously learned evaluation ...

48 A decade of reconfigurable computing: a visionary retrospective

R. Hartenstein
March 2001 **Proceedings of the conference on Design, automation and test in Europe**
Publisher: IEEE Press
Full text available: pdf(768.00 KB) Additional Information: full citation, references, citings, index terms

49 On rent's rule for rectangular regions

J. Dambre, P. Verplaetse, D. Stroobandt, J. Van Campenhout
March 2001 **Proceedings of the 2001 international workshop on System-level interconnect prediction**
Publisher: ACM Press
Full text available: pdf(272.25 KB) Additional Information: full citation, abstract, references, citings, index terms

A priori wirelength estimates are based on a terminal-gate relationship known as Rent's rule. Conventional models apply Rent's rule in 2D on square or diamond-shaped regions. However, more advanced applications of wirelength estimation require the use of Rent's rule on layout regions with different shapes. In this paper, we systematically study the layout Rent parameters of rectangular regions in a 2D layout medium. For this purpose, we derive a theoretical model for the pin versus gate rel ...

Keywords: Rent's rule, layout Rent parameters, rectangular layout region, wirelength distribution

50 Coarse grain reconfigurable architecture (embedded tutorial)

Reiner Hartenstein
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**
Publisher: ACM Press
Full text available: pdf(167.05 KB) Additional Information: full citation, abstract, references, citings, index

terms

The paper gives a brief survey over a decade of R&D on coarse grain reconfigurable hardware and related compilation techniques and points out its significance to the emerging discipline of reconfigurable computing.

51 The tangram framework (embedded tutorial): asynchronous circuits for low power

Joep Kessels, Ad Peeters
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**
Publisher: ACM Press

Full text available: pdf(255.11 KB) Additional Information: full citation, abstract, references, citings, index terms

Asynchronous CMOS circuits have the potential for very low power consumption, because they only dissipate when and where active. In addition they have favorable EMC properties, since they emit less energy, which in addition is evenly distributed over the spectrum. The Tangram framework supports the design of asynchronous circuits in a high-level programming language. Using this framework we have designed several chips, such as for instance for pagers and smart cards, which are clearly super ...

52 An RTL design-space exploration method for high-level applications

Peng-Cheng Kao, Chih-Kuang Hsieh, Allen C.-H. Wu
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**
Publisher: ACM Press

Full text available: pdf(312.59 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we present an RTL design-space exploration method for high-level applications. We formulate the RTL design-space exploration into a performance-driven module selection problem. We devise a dynamic-programming algorithm to solve the problem. We present an exploration flow by integrating commercial synthesis and layout tools with our proposed method. Experimental results have demonstrated that generating AT-curve for all modules is the most time consuming task in the design-spa ...

53 System level design research in an industrial setting (invited talks): IP reuse in the system on a chip era

Warren Savage, John Chilton, Raul Camposano
September 2000 **Proceedings of the 13th international symposium on System synthesis**
Publisher: IEEE Computer Society

Full text available: pdf(728.70 KB) Additional Information: full citation, abstract, references

Intellectual Property (IP) Reuse is one of the keys for System on a Chip (SoC) design productivity improvement. Although IP reuse has been explored both technically and as a business for many years, only recently systematic approaches based on EDA technology are starting to emerge in the marketplace. This paper gives an introduction to IP creation, IP conversion and the necessary infrastructure. We address the technical challenges and show that a strict quality based design methodology is the co ...

54 Composing contracts: an adventure in financial engineering (functional pearl)

Simon Peyton Jones, Jean-Marc Eber, Julian Seward
September 2000 **ACM SIGPLAN Notices , Proceedings of the fifth ACM SIGPLAN international conference on Functional programming ICFP '00**, Volume 35 Issue 9
Publisher: ACM Press

Full text available: pdf(642.59 KB) Additional Information: full citation, abstract, references, citings, index

terms

Financial and insurance contracts do not sound like promising territory for functional programming and formal semantics, but in fact we have discovered that insights from programming languages bear directly on the complex subject of describing and valuing a large class of contracts.We introduce a combinator library that allows us to describe such contracts precisely, and a compositional denotational semantics that says what such contracts are worth. We sketch an implementation of our combinator ...

55 Designing systems-on-chip using cores

Reinaldo A. Bergamaschi, William R. Lee
June 2000 **Proceedings of the 37th conference on Design automation**
Publisher: ACM Press

Full text available: pdf(88.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Leading-edge systems-on-chip (SoC) being designed today could reach 20 Million gates and 0.5 to 1 GHz operating frequency. In order to implement such systems, designers are increasingly relying on reuse of Intellectual property (IP) blocks. Since IP blocks are pre-designed and pre-verified, the designer can concentrate on the complete system without having to worry about the correctness or performance of the individual components. That is the goal, in theory. In practice, assembling on SoC ...

56 A current driven routing and verification methodology for analog applications

Thorsten Adler, Hiltrud Brocke, Lars Hedrich, Erich Barke
June 2000 **Proceedings of the 37th conference on Design automation**
Publisher: ACM Press

Full text available: pdf(182.57 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a new methodology for current driven routing and layout verification for analog applications used to avoid defects due to electromigration. The methodology presented uses a commercial simulator to calculate the current flow at all terminals of the analog circuit. Afterwards maximum currents per terminal are extracted and used as guidance for the Current Driven Router (CDR) which is capable of routing analog multiterminal signal nets with current driven wire widths.
Keywords: Steiner tree, current density, design methodology, electromigration, multiterminal signal nets, routing, verification

57 Multilevel cooperative search: application to the circuit/hypergraph partitioning problem

Min Ouyang, Michel Toulouse, Krishnaiyan Thulasiraman, Fred Glover, Jitender S. Deogun
May 2000 **Proceedings of the 2000 international symposium on Physical design**
Publisher: ACM Press
Full text available: pdf(201.09 KB) Additional Information: full citation, references

58 Graphical user interface of FIESTA—software for faults identification and estimation of testability of VLSI circuits

Mykola Blyzniuk, Taras Panchak, Wieslaw Kuzmicz, Witold Pleskacz
February 2000 **Proceedings of the symposium on Contemporary computing in Ukraine**
Publisher: ACM Press
Full text available: pdf(7.00 MB) Additional Information: full citation, abstract, index terms

We present the graphical user interface (GUI) of FIESTA software tools. It is based on the

proposed principles of open systems development. FIESTA was designed as UNIX application and works under Solaris 2.5.1. Graphical user interface of FIESTA has been developed with the use of Tel/Tk 8.2 design environment.

Keywords: faults identification, graphical user interface, software tools, usefulness of test vector components

59 New parallelization and convergence results for NC: a negotiation-based FPGA router

Pak K. Chan, Martine D. F. Schlag

February 2000 **Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(953.15 KB) Additional Information: full citation, abstract, references, citings, index terms

The negotiation-based routing paradigm has been used successfully in a number of FPGA routers. In this paper, we report several new findings related to the negotiation-based routing paradigm. We examine in-depth the convergence of the negotiation-based routing algorithm. We illustrate that the negotiation-based algorithm can be parallelized. Finally, we demonstrate that a negotiation-based parallel FPGA router can perform well in terms of delay and speedup with practical FPGA circui ...

60 CAD directions for high performance asynchronous circuits

Ken Stevens, Shai Rotem, Steven M. Burns, Jordi Cortadella, Ran Ginosar, Michael Kishinevsky, Marly Roncken

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Publisher: ACM Press

Full text available: pdf(124.02 KB) Additional Information: full citation, references, citings, index terms

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